DCS1800 Base Station Receiver Integrated in 0.25μm CMOS

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Abstract — **This paper describes the first CMOS chip implementation of a GSM base station receiver. This chip consists of two LNA's, switch, mixer, LO buffer amplifier/balun, and RF balun. A CMOS IF amplifier is packaged separately. The 0.25 μm CMOS receiver, biased at 3 V, meets DCS1800 specifications and achieves better linearity and noise figure than previously published BiCMOS receivers. Output IP3 (OIP3) of over 25 dBm was obtained for the complete receiver chain, with a noise figure of 3 dB, and gain of 25 dB. This is believed to be the highest OIP3 and lowest NF reported to date for a CMOS receiver that meets GSM base station specifications.**

I. Introduction

Digital cellular system (DCS) 1800 standard was introduced in Europe in early 1990's to provide more bandwidth for GSM users, which now comprise over two thirds of world cellular subscribers. Similarly to other cellular wireless standards, GSM Base Transceiver Station (BTS) specifications impose challenging sensitivity and linearity requirements on the receiver front-end, in comparison with user terminals [1]-[2]. While handsets receive and transmit only one channel at a time, a base station radio handles multiple channels simultaneously, and thus requires a higher dynamic range. Consequently, an RF receiver suitable for BTS applications must meet two demanding requirements: low noise figure (NF), and a high input and output third-order intercept points (IIP3 and OIP3). Typically base station radios use high performance but costly GaAs technology, with a low level of integration and a high number of external RF passive components [3]-[4]. However, it has recently been demonstrated that it is possible to meet GSM base station specifications using silicon BiCMOS technology in 900 and 1800 MHz bands [5]-[6]. While BiCMOS technology offers the convenience of providing both bipolar and MOSFET devices for circuit design, the bipolar module increases the number of process masks and processing cycle and hence the cost. CMOS solution would not only decrease the cost, but also open the possibility of integrating RF and digital parts of the radio on a standard CMOS process. CMOS technology used to be considered inferior to bipolar due to lower g_m/I ratio, and thus unsuitable for RF circuits. However, increased device speed, driven by demand for faster digital processors, has compensated for many drawbacks of CMOS devices. It has been demonstrated that CMOS devices can achieve minimum noise figure of under 0.5 dB [7], and CMOS LNA's can achieve NF comparable to that of bipolar circuits [8]-[10]. CMOS devices exhibit high linearity due to near square-law current versus voltage [11], and thus produce lower third-order intermodulation distortion than bipolar devices in BiCMOS technology [12]. CMOS devices are also natural candidates for switch implementation [13].

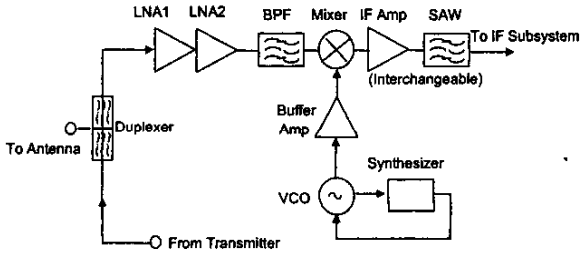

Fig. 1. Typical radio front-end architecture for base station receivers.

This paper describes the design and measured performance of the first reported base station receiver realized in a low-cost CMOS technology. This receiver, fabricated using Agere Systems (formerly Lucent Microelectronics) 0.25 μm CMOS process, meets DCS1800 base station specifications. Noise figure of 3 dB was achieved for the receiver chain with 25 dB of gain and over 25 dBm of OIP3. This is the highest OIP3 reported to date for an integrated receiver in CMOS technology.

II. Receiver Architecture

Base stations typically use a heterodyne receiver front-end architecture, as shown in Fig. 1. While there is still no commercially available integrated solution for filters, all other radio components can be integrated on a single chip. Using a similar architecture to BiCMOS chips reported in [5], the receiver described in this paper integrates two LNA's, switch, double balanced mixer [16], LO buffer amplifier, and RF balun on a single chip. IF amplifier was

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packaged separately to allow the reuse of this chip after channel select filters. Bipolar LNA's and LO buffer amplifier were replaced by CMOS circuits, to improve linearity and reduce the cost. Details of the design of these two circuits will be addressed in the following section.

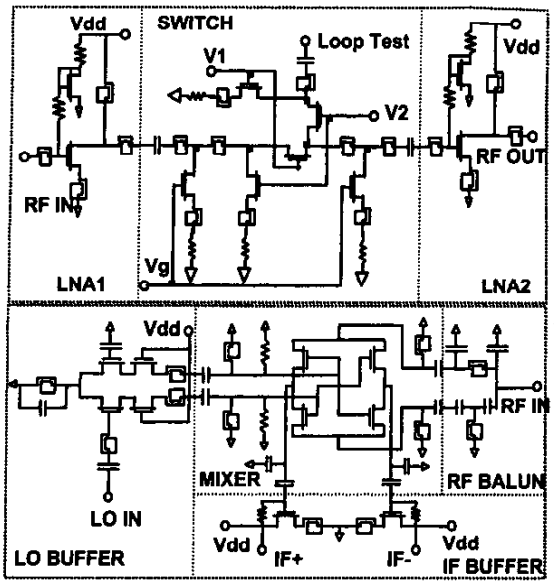

Fig. 2. Circuit schematic of DCS1800 receiver: LNA1, switch, LNA2, RF Balun, LO Buffer, Mixer, and IF amplifier.

Simplified schematic of the receiver chip is shown in Fig. 2. The LNA before mixer is partitioned into two stages, LNA1 and LNA2. The switch in between LNA's is used for a system loop test, and to bypass LNA1 when the external tower-top amplifier is used. This switch also provides a variable attenuation control to adjust receiver gain and linearity if necessary [13]. Output of LNA2 goes off chip to the power divider to provide diversity, and to image-reject filter. The filter output is connected to the mixer through the on-chip RF balun. The on-chip LO buffer amplifier converts single-ended LO input to differential output and amplifies its power level to drive the double balanced mixer. IF output of the mixer is amplified by IF buffer in front of the channel select SAW filter and IF sampling.

Gain partitioning of the receiver chain was critical to ensure high linearity without gain control, while minimizing noise figure. LNA1 and LNA2 were designed for the minimum gain that still provides sufficiently low NF for the whole chain. Gain was boosted instead at the IF stage with less penalty on receiver linearity. Passive resistive mixer [14] was chosen instead of commonly used Gilbert-cell mixer, for optimum linearity and noise performance. This type of mixer can be implemented with CMOS but not with bipolar devices. LO buffer amplifier is necessary to deliver 10-15 dBm of LO drive required by the passive mixer.

III. CMOS Implementation

All of the building blocks shown in Fig. 2 were integrated using Agere Systems 0.25 μm CMOS process. This process offers five metal levels, with 3μm thick top level metal for improved inductor Q. Top level metal was also used for RF signal routing whenever possible, as well as in the layout of CMOS devices, to minimize losses. Substrate resistivity was about 10 Ω/cm. Inductor Q values of around 10 were achieved for inductance of 1 to 12 nH. All inductors, including LNA input matching, were integrated on chip. Total chip size was about 10 mm^2. The die photo of DCS1800 integrated chip including LNA1, switch, LNA2, mixer, RF balun, and LO buffer is shown in Figure 3. Exposed pad TQFP-48 package [15] was used to provide a good RF ground, and reduce grounding inductance to below 0.5 nH.

While mixer, switch, and RF balun are similar to those reported in [5], CMOS LNA's and LO buffer design required special consideration.

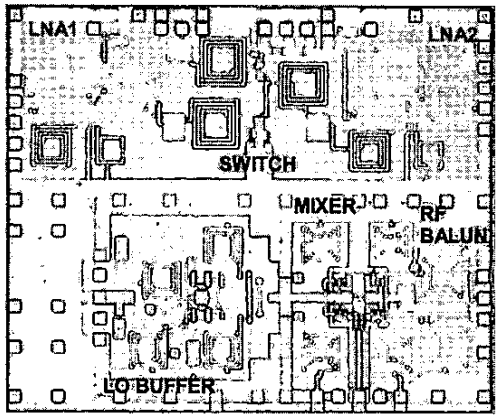

Fig. 3. Chip photograph. Chip size is 3.5 mm x 3.0 mm.

A. LNA

While CMOS amplifiers have demonstrated low-noise performance [9]-[10], high dynamic range is still a challenge. BiCMOS amplifier chip sets that meet both NF and linearity GSM BTS specifications were reported in [16]. Since bipolar devices require low bias current for low-noise performance, and a high bias current for high-linearity performance, LNA1 and LNA2 had to be designed as two different circuits for BiCMOS chip [5]. On the other hand, CMOS devices can achieve low noise

figure and high dynamic range simultaneously, making it possible to use the same amplifier for both stages, thus simplifying the design.

A single stage, common source configuration was chosen for optimum linearity and NF [17]. The device size was selected to provide best linearity and NF input match at the design frequency, without degrading gain significantly. This resulted in gate size of about 170 μm^2. Minimum NF (NF_{min}) of this large device was measured to be 0.5-0.8 dB at 1-2 GHz, for drain bias of 3 V, and drain current in the range of 10-60 mA. Since device NF_{min} is sufficiently low, it was possible to use series on-chip inductors for input matching and still meet NF specification. Degeneration inductance was added at the source terminal, to improve IIP3, and input and output return losses. A current mirror with smaller transistor size was used to set the gate bias voltage, and help with process and temperature compensation. With 3V bias voltage, bias current of 28 mA was chosen for best linearity and noise figure. However, these amplifiers can be biased at the much lower current, without significant performance degradation. With half the drain current, IIP3 is lowered only by about 1dB, and NF is increased by only about 0.2 dB. This makes CMOS amplifier performance very robust to changes in bias conditions due to process and temperature variations.

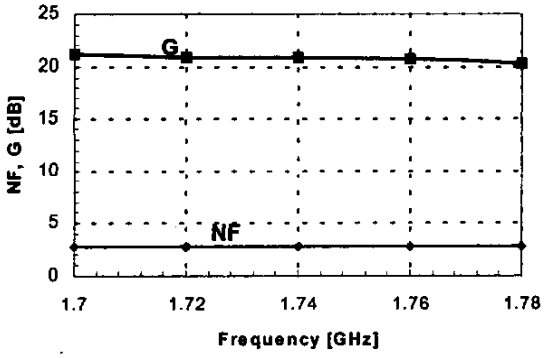

Fig. 4. LNA1/Switch/LNA2 noise figure and gain measured over DCS1800 bandwidth.

B. LO Buffer

The LO buffer amplifier converts single-ended LO input to differential output that drives the double-balanced mixer [5]. Current consumption is 75 mA with 3 V supply. The circuit is a differential amplifier with one input terminal AC grounded. The circuit topology is similar to the bipolar buffer amplifier reported in [18] with two modifications. First, the current source bias is removed from source coupled node, and current mirror is used to set the required bias voltage at the gate. Since there is no DC current flowing into gate, a very large resistor can be placed before gate to increase RF isolation. This is not practical in bipolar technology since base current is not zero. Second, since the current source is removed from the source coupled node, the power supply has enough headroom to support a cascode structure without degrading linearity. Cascode structure also provides very good isolation between output and input that makes impedance matching easier. An output impedance matching network and the LC resonator at coupled source node provide enhanced common mode rejection to keep the phase balance close to 180°. The amplifier provides a gain of about 15 dB. Both input and output are AC coupled.

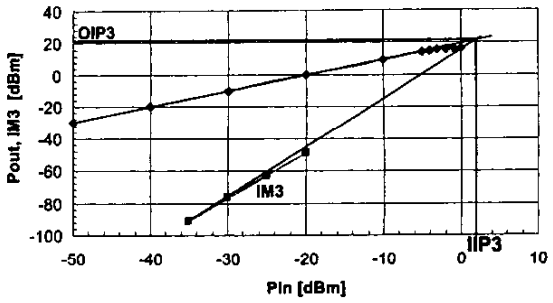

Fig. 5. LNA1/Switch/LNA2 output power and third order intermodulation product (IM3) as a function of input power.

IV. Measured Results

LNA1, switch, and LNA2 chain was evaluated in package, while other components were measured on-wafer. Receiver performance was then calculated by taking into account the losses of diversity power divider and image-reject filter. Noise figure and gain for LNA1, switch, and LNA2 is shown in Fig. 4 in DCS1800 band. Noise figure of 2.7 dB was achieved with 21 dB of gain over the whole bandwidth. Figure 5 shows output power and third order intermodulation product (IM3) as a function of input power for this stage, measured at 1.8 GHz. Third order intercept point was determined to be 1dBm at the input, and 22 dBm at the output, while 1 dB gain compression occurs at –4.5 dBm. Table I shows the performance summary for LNA1, switch, and LNA2 chain, as well as for the whole receiver. Receiver NF of 3 dB was achieved with 25 dB of gain. OIP3 of 25 dBm shows that CMOS receiver has better linearity than BiCMOS receiver [5]. While the total bias current of over 200 mA was used to obtain the best possible performance, receiver achieves

excellent NF and linearity even for half of that current. With IF amplifier current of 40 mA [5] instead of 90 mA, overall NF remains unchanged, while OIP3 decreases by less than 2dB.

V. Conclusion

The integrated RF receiver presented here achieves DCS1800 base station performance in a low cost 0.25μm silicon CMOS technology. This CMOS receiver has demonstrated better performance than previously published BiCMOS receivers, indicating that it is feasible to use CMOS technology for base stations radios. Silicon CMOS technology can reduce cost and size of base stations significantly and lead to the System-On-Chip (SOC) design, even for wireless standards with demanding RF specifications.

TABLE I

Performance Summary

	LNA1/SW LNA2	MIXER/ LO Buff.	IF Amp	Rx
G[dB]	21	-6.4	16.3	25.9
NF [dB]	2.7	6.4	1.2	3.0
P1dB [dBm]	-4.5	11.3	7.5	-5
IIP3 [dBm]	1	21.9	18.5	-0.7
OIP3 [dBm]	22	15.5	34.8	25.2
Idc[mA]	56	75	90	221

Acknowledgment

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